WHAT IS CLAIMED IS:

1. A method for storing data within a non-volatile memory of a memory system, the method comprising:

identifying a first block into which the data is to be stored;

obtaining an indicator associated with the first block;

determining when the indicator indicates that the data is to be encoded using a first algorithm;

encoding the data using the first algorithm when it is determined that the data is to be encoded using the first algorithm; and

writing the data encoded using the first algorithm into the first block.

2. The method of claim 1 further including:

encoding the data using a second algorithm when it is determined that the data is not to be encoded using the first algorithm; and

writing the data encoded using the second algorithm into the first block.

3. The method of claim 2 wherein the first algorithm is a 1-bit error correction code (ECC) algorithm and the second algorithm is a 2-bit ECC algorithm.

4. The method of claim 2 wherein the indicator is arranged to indicate when the block is a reclaimed block, wherein when the block is a reclaimed block, the indicator is further arranged to indicate that the data is to be encoded using the second algorithm.

5. The method of claim 2 wherein the indicator is arranged to indicate a number of times the block has been erased.

6. The method of claim 5 wherein determining when the indicator indicates that the data is to be encoded using the first algorithm includes:

determining when the indicator is less than a threshold value, wherein when the indicator is less than the threshold value, the data is to be encoded using the first algorithm.

7. The method of claim 2 wherein the indicator is arranged to indicate an approximately average number of times blocks within the non-volatile memory have been erased.

8. The method of claim 2 wherein the indicator is stored in a data structure, the data structure being substantially separate from the first block, and obtaining the indicator associated with the block includes obtaining the indicator from the data structure.

9. The method of claim 1 wherein the non-volatile memory is a flash memory.

10. The method of claim 9 wherein the flash memory is one of a NAND flash memory and an MLC NAND flash memory.

11. A method for reading data within a non-volatile memory of a memory system, the method comprising:

identifying a first block from which data is to be read;

obtaining an indicator associated with the first block;

determining when the indicator indicates that the data stored in the first block has encoded using a first algorithm; and

decoding the data using the first algorithm when it is determined that the data has been encoded using the first algorithm.

12. The method of claim 11 further including:

decoding the data using a second algorithm when it is determined that the data has not been encoded using the first algorithm.

13. The method of claim 12 wherein the first algorithm is a 1-bit ECC algorithm and the second algorithm is a 2-bit ECC algorithm.

14. The method of claim 12 wherein the indicator is arranged to indicate when the block is a reclaimed block, wherein when the block is a reclaimed block, the indicator is further arranged to indicate that the data has been encoded using the second algorithm.

15. The method of claim 12 wherein the indicator is arranged to indicate a number of times the block has been erased.

16. The method of claim 15 wherein determining when the indicator indicates that the data has been encoded using the first algorithm includes:

determining when the indicator is less than a threshold value, wherein when the indicator is less than the threshold value, the data has been encoded using the first algorithm.

17. The method of claim 12 wherein the indicator is arranged to indicate an approximately average number of times physical blocks of the non-volatile memory have been erased.

18. The method of claim 12 wherein the indicator is stored in a data structure, the data structure being substantially separate from the first block, and obtaining the indicator associated with the block includes obtaining the indicator from the data structure.

19. The method of claim 11 wherein the non-volatile memory is a flash memory.

20. The method of claim 19 wherein the flash memory is one of a NAND flash memory and an MLC NAND flash memory.

21. A memory system comprising:

a non-volatile memory including a plurality of blocks, the plurality of blocks including a first block;

code devices for identifying the first block into which data is to be stored;

code devices for obtaining an indicator associated with the first block;

code devices for determining when the indicator indicates that the data is to be encoded using a first algorithm;

code devices for encoding the data using the first algorithm when it is determined that the data is to be encoded using the first algorithm;

code devices for writing the data encoded using the first algorithm into the first block; and

a memory area that stores the code devices.

22. The memory system of claim 21 further including:

code devices for encoding the data using a second algorithm when it is determined that the data is not to be encoded using the first algorithm; and

code devices for writing the data encoded using the second algorithm into the first block.

23. The memory system of claim 22 wherein the first algorithm is a 1-bit ECC algorithm and the second algorithm is a 2-bit ECC algorithm.

24. The memory system of claim 22 wherein the indicator is arranged to indicate when the block is a reclaimed block, wherein when the block is a reclaimed block, the indicator is further arranged to indicate that the data is to be encoded using the second algorithm.

25. The memory system of claim 22 wherein the indicator is arranged to indicate a number of times the block has been erased.

26. The memory system of claim 25 wherein the code devices for determining when the indicator indicates that the data is to be encoded using the first algorithm include:

code devices for determining when the indicator is less than a threshold value, wherein when the indicator is less than the threshold value, the data is to be encoded using the first algorithm.

27. The memory system of claim 21 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.

28. A memory system comprising:

a non-volatile memory including a plurality of blocks, the plurality of blocks including a first block, the first block including data;

code devices for identifying the first block;

code devices for obtaining an indicator associated with the first block;

code devices for determining when the indicator indicates that the data has been encoded using a first algorithm;

code devices for decoding the data using the first algorithm when it is determined that the data has been encoded using the first algorithm; and

a memory area that stores the code devices.

29. The memory system of claim 29 further including:

code devices for decoding the data using a second algorithm when it is determined that the data has not been encoded using the first algorithm.

30. The memory system of claim 30 wherein the first algorithm is a 1-bit ECC algorithm and the second algorithm is a 2-bit ECC algorithm.

31. The memory system of claim 30 wherein the indicator is arranged to indicate when the block is a reclaimed block, wherein when the block is a reclaimed block, the

indicator is further arranged to indicate that the data has been encoded using the second algorithm.

32 33. The memory system of claim 30 wherein the indicator is arranged to indicate a number of times the block has been erased.

33 34. The memory system of claim 33 wherein the code devices for determining when the indicator indicates that the data has been encoded using the first algorithm include:

code devices for determining when the indicator is less than a threshold value, wherein when the indicator is less than the threshold value, the data has been encoded using the first algorithm.

34 35. The memory system of claim 29 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.

35 36. A memory system comprising:

a non-volatile memory including a plurality of blocks, the blocks including a first block and a second block, the first block including a first set of contents encoded using a first algorithm, the second block including a second set of contents encoded using a second algorithm, wherein the non-volatile memory further includes a data structure that is arranged to indicate that the first set of contents is encoded using the first algorithm and that the second set of contents is encoded using the second algorithm;

code devices for accessing the data structure, wherein the code devices for accessing the data structure include code devices for determining that the first set of contents is encoded using the first algorithm and code devices for determining that the second set of contents is encoded using the second algorithm; and

a memory area that stores the code devices.

36 37. The memory system of claim 36 wherein the first algorithm is a 1-bit ECC algorithm and the second algorithm is a 2-bit ECC algorithm.

37/38. The memory system of claim 37 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.

38/39. A memory system comprising:

a non-volatile memory that includes a first block into which data is to be stored;

means that identify the first block;

means that obtain an indicator associated with the first block;

means that determine when the indicator indicates that the data is to be encoded using a first algorithm; and

means that encode the data using the first algorithm when it is determined that the data is to be encoded using the first algorithm.

39/40. The memory system of claim 39 further including:

means that encode the data using a second algorithm when it is determined that the data is not to be encoded using the first algorithm; and

means that write the data encoded using the second algorithm into the first block.

40/41. The memory system of claim 40 wherein the first algorithm is a 1-bit ECC algorithm and the second algorithm is a 2-bit ECC algorithm.

41/42. The memory system of claim 39 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.

42/43. A memory system comprising:

a non-volatile memory that includes a first block from which data is to be read;

means that identify the first block;

means that obtain an indicator associated with the first block;

means that determine when the indicator indicates that the data stored in the first block has encoded using a first algorithm; and

means that decode the data using the first algorithm when it is determined that the data has been encoded using the first algorithm.

43/44. The memory system of claim 43 further including:

means that decode the data using a second algorithm when it is determined that the data has not been encoded using the first algorithm.

44/45. The memory system of claim 44 wherein the first algorithm is a 1-bit ECC algorithm and the second algorithm is a 2-bit ECC algorithm.

45/46. The memory system of claim 43 wherein the non-volatile memory is one of a NAND flash memory and an MLC NAND flash memory.